Frame grabbers

Matrox **Helios eD/XD**

64-bit LVDS/RS-422 frame grabber with powerful pre-processing capabilities.

Key features

- x4 PCIe™ (eD) or PCI-X® (XD) long card
- 64-bit LVDS or RS-422 interface
- acquires up to 480 MB per second
- 256 MB of DDR SDRAM memory
- performs complete image reconstruction from multi-tap frame and line-scan cameras
- over 5 GB per second of memory bandwidth
- powerful pre-processing core capable of up to 100 BOPS[1]
- up to 1 GB per second of I/O bandwidth to host PC
- serial communication ports can be mapped as PC COM ports
- support for rotary encoders with quadrature output
- programmed using Matrox Imaging Library (MIL) sold separately
- supports 32/64-bit Microsoft® Windows® XP/Vista® and 32/64-bit Linux®
- royalty-free redistribution of MIL's image processing module

Wide interface and more

Matrox Helios eD/XD is a high-performance LVDS/RS-422 frame grabber. It fully exploits PCIe™/PCI-X® technology to deliver unprecedented video capture rates for a single-board solution and can easily accommodate the most demanding video sources. A proprietary ASIC, designed by Matrox, combines a PCI-X controller with a powerful processor core to alleviate the host CPU from image formatting and pre-processing tasks. These features provide the Matrox Helios eD/XD with the power and flexibility needed for vision applications of today and tomorrow.

64-bit LVDS/RS-422 interface

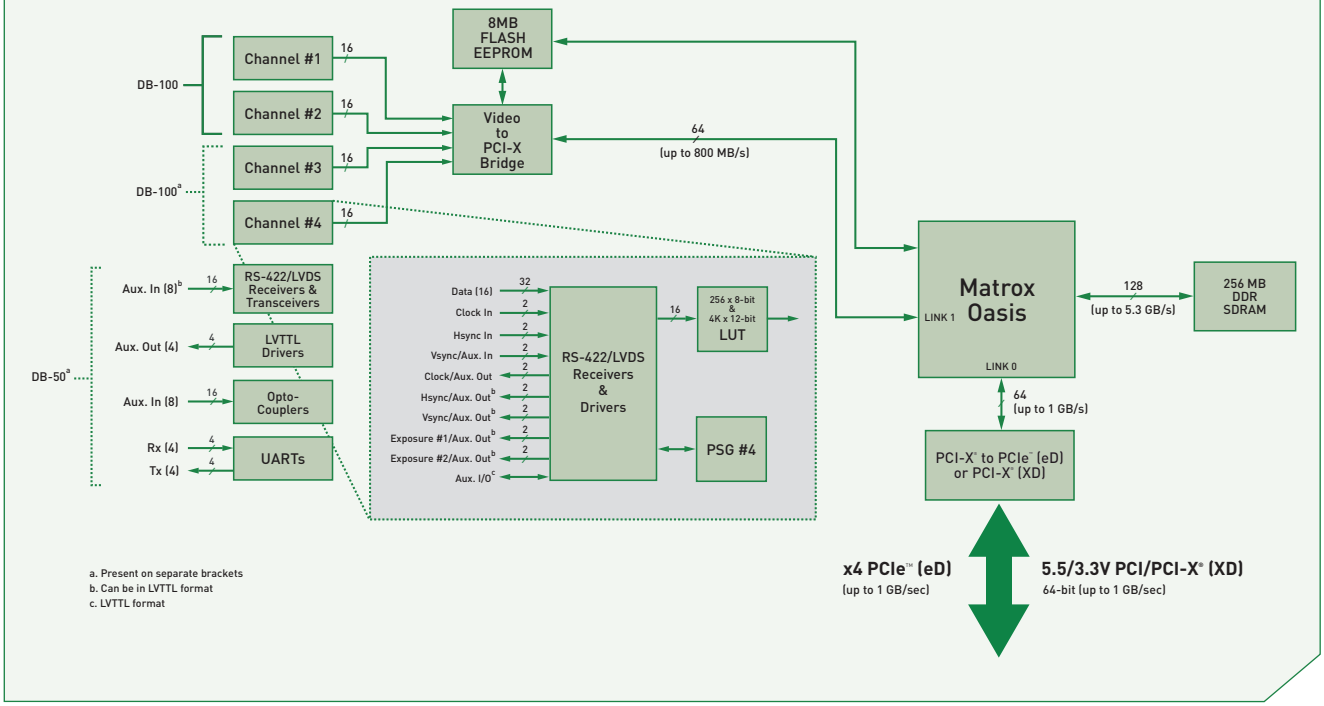
Designed to support legacy scientific, industrial and medical imaging devices, the Matrox Helios eD/XD features four completely independent 16-bit wide inputs. These inputs can be configured to acquire from two, four and eight-tap monochrome sources as well as RGB sources. The Matrox Helios eD/XD also includes an internal video generator for troubleshooting installation and operation.

Choice of high-performance host bus interfaces

Four lane (x4) PCIe™ and PCI-X® are the interfaces used to connect to the host PC on the Matrox Helios eD and Matrox Helios XD boards respectively. PCIe™ is the follow-on to conventional PCI and PCI-X®. Version 1.x of PCIe™ operates at 2.5 GHz to deliver a peak bandwidth of 1GB/sec over a x4 implementation. PCI-X® is a high-performance backwards-compatible enhancement to conventional PCI. Version 1.0a of PCI-X® specifies a 64-bit physical connection running at speeds of up to 133 MHz resulting in a peak bandwidth of up to 1 GB per second.

MATROX IMAGING

Matrox Helios eD/XD



a. Present on separate brackets
b. Can be in LVTTL format
c. LVTTL format

State-of-the-art Matrox Oasis ASIC

The Matrox Imaging designed Oasis ASIC is the pivotal component of the Matrox Helios eD/XD. A high-density chip, the Matrox Oasis integrates a Links Controller, main memory controller and Pixel Accelerator.

Pixel Accelerator

The Pixel Accelerator (PA) is a parallel processor core, which considerably accelerates neighborhood, point-to-point and LUT mapping operations. It consists of an array of 64 processing elements all working in parallel. Each processing element has a multiply-accumulate (MAC) unit and an arithmetic-logic unit (ALU).

The MAC unit is capable of performing a single 16-bit by 16-bit, two 8-bit by 16-bit or four 8-bit by 8-bit multiplies with 40-bit accumulation per cycle for convolution operations. The 40-bit accumulator guarantees no overflow situation for a 16 by 16 kernel with 16-bit coefficients and data. In addition, the PA architecture allows symmetrical kernels to be processed four times faster. The MAC unit is also able to perform up to four minimum or maximum operations per cycle for grayscale morphology operations.

The ALU can execute a wide variety of arithmetic and logical operations. It can be programmed to execute a sequence of 256 instructions per pixel at one instruction per cycle reducing the amount of memory accesses and further accelerating memory I/O-bound sequences. The PA can accept up to four source buffers[2] and output to four destination buffers allowing several operations to be performed at once or in a single pass (e.g., four images can be averaged in one pass). Operating at a core frequency of 167 MHz enables the PA to carry out up to 100 BOPS[1] (i.e., process over two billion pixels per second).

Memory controller

The Matrox Oasis includes a very efficient main memory controller for managing the 128-bit wide interface to DDR SDRAM memory. Operating at 167 MHz, the DDR SDRAM memory and controller combine to deliver a memory bandwidth in excess of 5 GB per second. Such ample memory bandwidth allows the Matrox Helios eD/XD to comfortably handle demanding video I/O while maintaining PA performance even for memory I/O-bound operations.

Links Controller

The Links Controller (LINX) is the router that manages all data movement within the Matrox Helios eD/XD. It oversees the transfer of image data from the frame grabber section to onboard memory for pre-processing and from onboard memory to the host PC including display. Image data can be subject to various formatting operations including plane separation on input and merging on output, input cropping, input and output sub-sampling (1 to 16), and independent control of horizontal and vertical scanning direction. The latter is particularly useful for reconstructing a proper image from a camera whose readout requires multiple taps, each with different scanning directions.

Field-proven application development software

Matrox Helios eD/XD is supported by the Matrox Imaging Library (MIL), a comprehensive collection of software tools for developing industrial imaging applications. MIL features interactive software and programming functions for image capture, processing, analysis, annotation, display and archiving. These tools are designed to enhance productivity, thereby reducing the time and effort required to bring your solution to market. Refer to the MIL datasheet for more information.

MIL's image processing module, when used with the Matrox Helios eD/XD, comes with royalty-free redistribution rights. The image processing module, which includes functions for basic arithmetic, logic, LUT mapping, per pixel gain and offset, morphology, spatial filtering, statistics, temporal filtering and threshold, is fully optimized for the PA[3]. Support for custom PA functions is also available on demand and upon evaluation.

Specifications

Hardware

- x4 PCIe™ long card or PCI/PCI-X® long card with universal 64-bit card edge connector (64-bit 33/66 MHz 5/3.3V PCI and 64-bit 66/100/133 MHz PCI-X)
- 256 MB of 167 MHz DDR SDRAM main memory
- four independent video inputs with
  - 16-bit wide LVDS or RS-422 interface
  - acquisition rates up to 60 MHz for LVDS and 32 MHz for RS-422
  - 256 x 8-bit and 4K x 12-bit LUTs
  - LVDS/RS-422 clock, hsync and vsync/auxiliary inputs
  - five LVDS/RS-422 configurable auxiliary outputs (four can be LVTTL)
  - three LVTTL configurable auxiliary I/Os
  - serial communication port
- can be configured to acquire from
  - four single-tap 8 to 16-bit or dual-tap 8-bit monochrome sources
  - two dual-tap 10 to 16-bit or four-tap 8-bit monochrome sources
  - single four-tap 10 to 16-bit or eight-tap 8-bit monochrome source
  - two 8-bit RGB sources
  - single 10 to 16-bit RGB source
- supports frame and line-scan video sources
- eight LVDS/RS-422 configurable auxiliary inputs (two can be LVTTL)
- four LVDS/RS-422 configurable auxiliary outputs
- eight opto-isolated configurable auxiliary inputs
- internal video generator for diagnostics

Dimensions and environmental information

- 31.4 L x 10.7 H x 1.73 W cm (12.4" x 4.2" x 0.68") from bottom edge of goldfinger to top edge of board and without bracket and retainer
- power consumption (typical): 3.1A @ 5V or 18.15W total
- operating temperature: 0°C to 55° C (32° F to 131° F)
- ventilation requirements: 50 LFM (linear feet per minute) over board(s)
- relative humidity: up to 95% (non-condensing)
- FCC class B
- CE class B
- RoHS-compliant

Software drivers

- Matrox Imaging Library (MIL) drivers for 32/64-bit Microsoft® Windows® XP/Vista®
- MIL drivers for 32/64-bit Linux®

Ordering Information

Hardware

Part number	Description
HEL 2M QDL *or* R*[4]	PCI-X® 64-bit LVDS or RS-422 frame grabber with 256 MB DDR SDRAM and cable adapter boards.
HEL 2M QDL *or* R E*[4]	x4 PCIe™ 64-bit LVDS or RS-422 frame grabber with 256 MB DDR SDRAM and cable adapter boards.

Software

Refer to MIL datasheet.

Cable

Part number	Description
DBHD100-TO-OPEN	3 m (10') high density DB-100 to open end cable for LVDS/RS-422 frame grabber module (requires customization).

Note:

1. Billion operations per second.
2. Only one source buffer for MAC unit.
3. Accelerated functions include MbufBayer (bilinear interpolation) MimArithMultiple(M_OFFSET_GAIN, M_WEIGHTED_AVERAGE, M_MULTIPLY_ACCUMULATE), MimArith(M_ADD, M_ADD_CONST, M_SUB, M_SUB_CONST, M_SUB_ABS, M_MULT, M_MULT_CONST, M_CONST_SUB, M_AND, M_NAND, M_OR, M_XOR, M_NOR, M_XNOR, M_NOT, M_AND_CONST, M_NAND_CONST, M_OR_CONST, M_XOR_CONST, M_NOR_CONST, M_XNOR_CONST, M_NEG, M_ABS, M_MIN, M_MIN_CONST, M_MAX, M_MAX_CONST), MimResize(with specific factors), MimDilate(), MimErode(), MimThin(), MimThick(), MimDistance(), MimConnectMap(), MimMorphic(M_DILATE, M_ERODE, M_THICK, M_THIN, M_MATCH), MimConvolve(M_SMOOTH, M_SHARPEN, M_VERT_EDGE, M_HORIZ_EDGE, M_LAPLACIAN_EDGE, M_EDGE_DETECT), MimLutMap(8-bit), MimShift(), MimBinarize(), MimClip(), MimConvert(M_YUV16_TO_RGB, M_RGB_TO_YUV16, M_RGB_TO_L, M_L_TO_RGB, M_RGB_TO_Y), MimFlip(), MimFindExtreme(), MimCountDifference() and ActiveMIL equivalents.
4. Contact local representative or Matrox Imaging Sales for availability.

Corporate headquarters:
Matrox Electronic Systems Ltd.
1055 St. Regis Blvd.
Dorval, Quebec H9P 2T4
Canada
Tel: +1 (514) 685-2630
Fax: +1 (514) 822-6273

For more information, please call: 1-800-804-6243 (toll free in North America) or (514) 822-6020
or e-mail: imaging.info@matrox.com or http://www.matrox.com/imaging